Feature-based 3D Process Planning for MEMS Fabrication

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Abstract:
With the rapid growth of MEMS technology and market, computer-aided design and process planning systems are strongly required for an appropriate division of labor between MEMS design and its fabrication. The purpose of this study is to develop a new process planning system for MEMS devices for non-expert MEMS designers. The system can treat a 3D MEMS device model which has complex layered structure made of multiple materials as a solid model, and has three characteristic planning functions. In process extraction function, all feasible fabrication processes are exhaustively derived from a 3D device model. In geometry estimation function, a 3D geometry of the device actually fabricated by the derived process is estimated. And in associative modification function, the original process parameters can be associatively modified along with the dimensional change of the device to obtain the final consistent combination of the device and the process. The fabrication features in the device model provide clues to finding precedence in layer fabrication sequence. Two case studies indicated that the derived process plans and the device model geometry were plausible.

Keywords: MEMS, Process Planning, CAD, Feature Recognition

1. Introduction

MEMS stand for micro-electro-mechanical systems and have been successfully used as micro-engineering devices such as pressure, inertial and flow sensors, micro scanners, printer heads and lab-on-chips. MEMS devices have multi-layer structures fabricated using conventional integrated circuit processes, such as lithography, deposition and etching, together with a broad range of specially developed micro-machining technologies[1]. Therefore, MEMS devices designers originally need to have deep knowledge of the fabrication processes and the limitations placed on the device geometry.

On the other hand, with the rapid growth of the MEMS market, the separation of the devices design from its fabrication is increasing to enable an appropriate division of labor in MEMS industries[2]. Under the circumstances, even non-expert MEMS designers who do not necessarily have thorough knowledge of the fabrication processes need to be responsible for manufacturability of the device in early design stage. But it is generally difficult for the non-expert designers to correctly judge whether a given MEMS device structure can be fabricated well or not by taking all fabrication processes and their limitations into account.

So, computer-aided process planning systems for non-expert MEMS designers are strongly expected in the design stage of MEMS to solve the problem. We first interviewed experts involved in MEMS manufacturing and research on the functional requirements for the process planning system and finally found that the system has to fulfill the following four requirements.

1) 3D modeling of layered device geometry

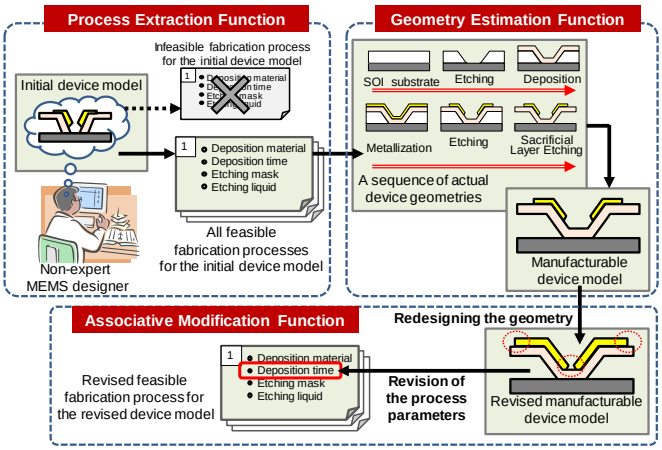


Figure 1 The proposed process planning system

Since MEMS devices have complex 3D overlaid layer structures composed of different materials, a 3D geometric model should be used to represent the layered geometry.

2) Discovering feasible process plans

Since device geometry has strong geometric limitations due to its layer-by-layer fabrication principle, original MEMS device geometry created by non-expert designers will often not be made as it is. In this case, the planning system should try to discover feasible process plans where a device with a little different geometry from the original one but similar to it can be reliably manufactured.

3) Estimating a 3D manufacturable device geometry

When any feasible process plan is found, the device geometry may become the one different from the original. So in the planning system, the 3D device

geometry actually made by the feasible plan has to be estimated. This function helps the designer differentiate the manufacturable device geometry from the original one.

4) Keeping the consistent association between feasible process plan and manufacturable device geometry
In MEMS, interdependency between manufacturable device geometry and feasible process is strong, so the designer has to keep their right consistency even when the device geometry needs to be revised.

The objective of this study is to develop a new process planning system for MEMS fabrication for non-expert MEMS designers which fulfill the above requirements. In our system, a 3D MEMS device geometry which has a complex layered structure made of multiple materials is expressed as a solid model called a *device model*. As shown in **Fig.1**, the system has three characteristic planning functions; process extraction function, geometry estimation function and associative modification function. In the process extraction function, all feasible fabrication processes and their photoresist masks can be exhaustively derived from the device model. In the geometry estimation function, a sequence of 3D geometries of the device actually made by the feasible process can be generated. Finally, in the associative modification function, the derived process parameters are first linked to the dimensional parameters of the device model, and then the process parameters can be automatically revised according to a change in dimensional parameters of the device model in redesign. The combination of the three functions enables non-expert MEMS designers to efficiently discover manufacturable and easier-to-fabricate device geometry as well as feasible fabrication processes.

2. Related Work

The computer-aided design systems for MEMS have been already commercialized. The main functions of the design systems are FEM/BEM-based electro-mechanical simulation of devices and the photoresist etching process simulation. In the process simulation, 3D device model is generated from the process sequences and the photoresist mask geometries[3,4]. These functions are implemented in integrated commercial tools like[5,6]. However, the systems lacked process planning ability where the process sequence and mask geometries can be generated from the device model in reverse.

On the other hand, relatively small numbers of computer-aided process planning systems for MEMS have been studied as basic research. Jawalkar et al. [7] developed a planning system based on the graph-based model which expresses the layer structure of the device. However, in their model, the relationship between the contiguous layers is only expressed, and 3D geometry of the layers in the device was not represented at all.

The system developed by Cho et al. [8] utilized a 3D device model and could derive a set of process sequences and the mask geometries from the connectivity. But they

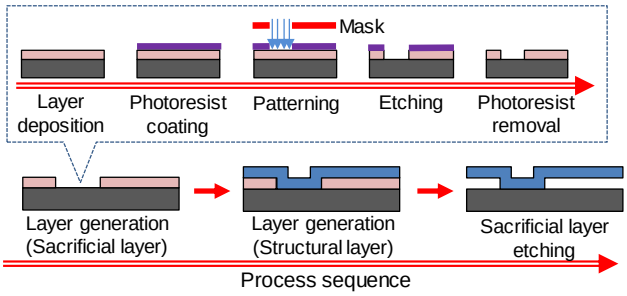


Figure 2 Surface micromachining process

over-simplified the model where all layers in the device were made of a single material, so feasibility of the derived processes was not necessarily guaranteed, and manufacturable device geometry could not be estimated.

An advanced process planning system was developed by Li et al.[9] where process features could be recognized from a 3D device model, and all potential process sequences could be extracted based on the features. The manufacturability of the initial device geometry could be locally checked. However, they also assumed the device was made of a single material, so their process sequence might include non-manufacturable or inefficient processes. Moreover their system could not estimate the actual 3D device geometries generated by the feasible process. Our research group also proposed the feature-based process planning system[10] where all feasible process sequences are derived from the 3D device models with different materials. However, the system also has the same problems as that of [9].

Li et al[11] recently proposed an integrated process planning system where feasible process plans could be found from the device model with detail shapes, micro-fabrication process could be simulated, and variational propagation between feasible process plan and manufacturable device geometry and mask geometries is realized. However, the process planning method still had the disadvantage similar to [9], and the technical details were not stated in the paper.

Therefore, any process planning system for MEMS device which meets the above four requirements has not been realized so far.

3. Process Assumptions and Device Model

3.1 Assumptions about MEMS process

In developing the process planning system, we made several assumptions about MEMS fabrication process.

Basically, only the surface micromachining is considered in the system. Moreover, we only consider that one side of the substrate is machined. The device geometry is simplified so that the layer shape consists only of horizontal and vertical faces. Different materials can be used in different layers in a device.

Fig.2 shows an example of the general fabrication process of the surface micromachining. A process consists of several process steps each of which includes the layer deposition, photoresist coating, patterning with a photoresist mask, etching and photoresist removal. The

hollow structure can also be made by inserting and removing sacrificial layers.

In the layer deposition, only the conformal deposition is considered where the deposition thickness along horizontal direction is assumed to be proportional to the vertical one. In the etching process, we assume that only one material becomes eroded, photoresists remains completely, etching proceeds ideally vertical to the substrate surface, and side-etch does not occur. The sacrificial layer assumed to be removed by one etching process while keeping the structural layers unchanged.

3.2 Representation of the device model

An initial MEMS device model SM_{init} which has layer-by-layer structures made of multiple materials is defined as a solid model in Eq.(1).

$$SM_{init} = \langle\ S,\ F,\ E,\ mat_s\ \rangle \tag{1}$$

where, S is a set of solid bodies of one connected layer made of a single material, F a set of faces and E a set of edges in the solid bodies in S. $mat_s : S \rightarrow M_n$ is a material of a deposited layer where M_n is a set of material names. A face $f \in F$ has its normal vector $\mathbf{n}(f)$, and an edge $e \in E$ has the concave-convex attribute $c(e) \in \{convex,\ concave\}$.

In the device model SM, it is assumed that the top surface of the substrate $f_0 \in F$ is aligned horizontally such as $\mathbf{n}(f_0) = (0,0,1)$, and all device layers except for the substrate are placed in a limited space $V_{dev} = \{(x,y,z) \mid x \in [-a,a], y \in [-b,b],\ z \in [0,\alpha]\}$ above f_0.

4. Process extraction function

4.1 Process extraction Strategy

In the MEMS fabrication process, a device is made by repeatedly depositing and etching the material layers. So a correct order of the layer deposition and etching has to be derived as a feasible process sequence from the device model in the process extraction function.

To derive the process, *fabrication features* are first extracted as clues to identifying precedence in a layer deposition order. As shown in **Fig.3**, a fabrication feature is a set of connected faces and edges placed in between two contiguous layers or in between a layer and a space. The overlay relationship among the fabrication features gives the layer deposition precedence. All feasible processes which agree with the precedence are exhaustively extracted in the function.

The process extraction consists of five steps; 1) All fabrication features are extracted from the device model, 2) A projection overlay relationship among the fabrication features is recognized, 3) A deposition precedence graph of the fabrication features is generated so that it agree with the projection overlay relationship, 4) A process tree is generated to represent all feasible processes sequences and the deposition states of the device, and 5) The process parameters of the feasible processes are extracted.

4.2 Extracting the fabrication features

First, the system extracts all fabrication features from the device model. A *fabrication feature* consist of connected *process features*, while a *process feature* consists of connected three faces and two edges placed between two solid bodies in a device model. A set of process features PF is defined as Eq.(2).

$$PF = \left\{ \left(\begin{matrix} f^t, f^m, f^b, \\ e^{tm}, e^{bm} \end{matrix} \right) \middle| \begin{matrix} f^t, f^m, f^b \in F(s_k), \\ e^{tm}, e^{bm} \in E(s_k),\ z(e^{tm}) < z(e^{bm}) \\ e^{tm} = f^t \cap f^m,\ e^{bm} = f^b \cap f^m, \\ \boldsymbol{n}(f^t) = -\boldsymbol{z},\ \boldsymbol{n}(f^b) = \pm\boldsymbol{z}, \\ \boldsymbol{n}(f^m) = p\boldsymbol{x} + q\boldsymbol{y},\ s_k \in S \end{matrix} \right\} \tag{2}$$

where $F(s_k)$ and $E(s_k)$ are a set of faces and edges included in a solid body of a layer $s_k (\in S)$. $e^i (= f^j \cap f^k)$ expresses that faces f^j and f^k share an edge e^i. f^t, f^m and f^b are respectively called *top face*, *middle face* and *bottom face*, and e^{tm} and e^{bm} are horizontal edges called *top edge* and *bottom edge*. $z(e^k)$ is a z coordinate of a horizontal edge e^k, $\boldsymbol{n}(f^j)$ a normal vector of a face f^j, $\boldsymbol{x}, \boldsymbol{y}$ and $\boldsymbol{z}$ the unit vector along x, y and z axes, and p and q arbitrary real numbers. All faces and edges which satisfy Eq.(2) are extracted as the process features.

Then, as shown in **Fig.4**, the process feature type $type_{pf}(p_f)$ is determined for each feature $p_f (\in PF)$ based on the concave-convex attribute of their edges $c(e^{tm})$ and $c(e^{bm})$ as Eq.(3).

$$type_{pf}(p_f) = \begin{cases} bend & \left(\begin{matrix} c(e^{tm}) = concave \\ \wedge\ c(e^{bm}) = convex \end{matrix} \right) \\ side\_pocket & \left(\begin{matrix} c(e^{tm}) = concave \\ \wedge\ c(e^{bm}) = concave \end{matrix} \right) \end{cases} \tag{3}$$

Afterward, the following four attributes are assigned to each process feature:

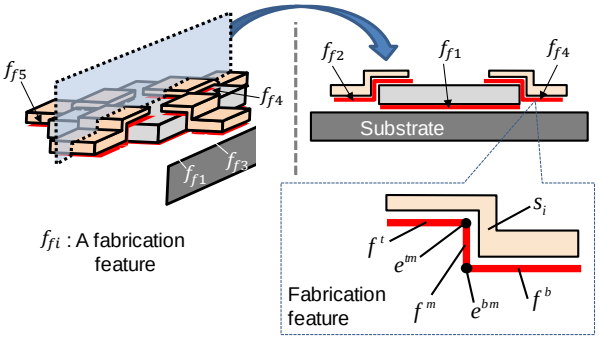


Figure 3 Fabrication feature

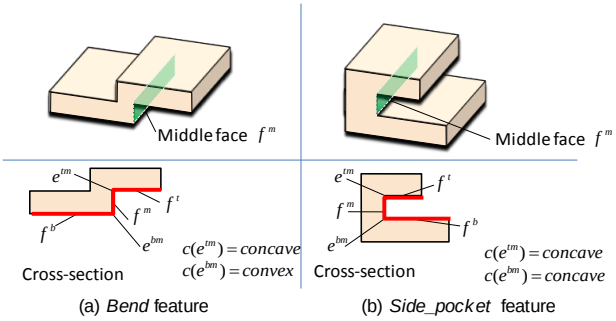


Figure 4 Process feature type

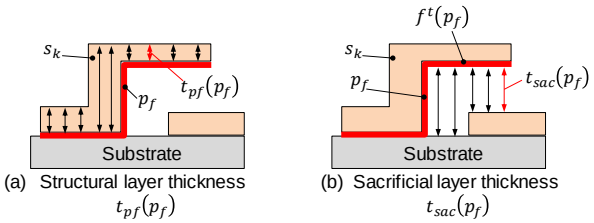


Figure 5 Deposition and sacrificial layer thickness

1) Material ($mat_{pf} : PF \rightarrow M_n$)
The material a process feature p_f is made identical to the one of the layer s_k which p_f belongs to.
2) Deposition thickness ($t_{pf} : PF \rightarrow R^+$)
As shown in **Fig.5(a)** the deposition thickness of the feature p_f represents the minimum vertical thickness in the layer s_k .
3) Sacrificial layer flag ($sac_{pf} : PF \rightarrow \{true, false\}$)
As shown in **Fig.5(b)**, the sacrificial layer attribute indicates whether an open space exists right below the *top face* of the process feature, and shows that a sacrificial layer must be deposited before making p_f.
4) Sacrificial layer thickness ($t_{sac} : PF \rightarrow R^+$)
If $sac_{pf}(p_f) = true$, the sacrificial layer thickness is evaluated and attached to p_f. As shown in **Fig.5(b)**, the attribute shows the minimum distance along z direction between a top face of the feature $f^t(p_f)$ and a face of the other structural layer which is placed below $f^t(p_f)$ and has a projection overlay relationship with p_f.

After that, a *fabrication feature* is generated from the process features. A fabrication feature is a set of connected process features which can be fabricated only by one deposition operation.

Before building the fabrication feature, as shown in **Fig.6**, a solid body including the side pocket feature is split into two bodies by cutting it with a plane identical to the bottom face of the feature. As a result, a new bend feature and a simple face are generated in the upper and lower bodies respectively.

Finally, as shown in **Fig.7**, the process features are

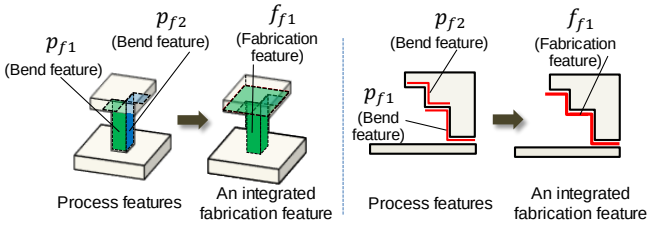


Figure 6 Splitting a side pocket feature

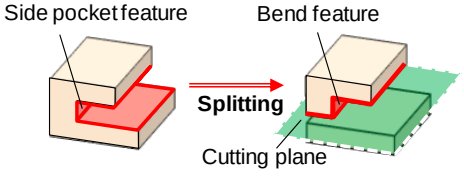


Figure 7 Process features and a fabrication feature

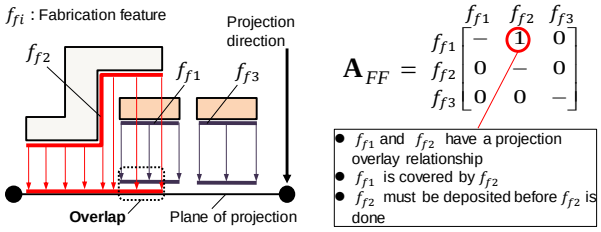


Figure 8 Deposition and sacrificial layer thickness

integrated to make a fabrication feature if two process features have at least one common face. By repeating the integration until no common face exists among the process features, a set of fabrication features are completed. At last, the attributes of the material, deposition thickness, sacrificial layer flag and sacrificial layer thickness of the fabrication feature are inherited from the ones of the base process features.

4.3 Recognizing the projection overlay relationship

After finding the fabrication features, the *projection overlay relationship* among the fabrication features is recognized, and the result is stored in a *projection overlay relationship matrix*.

The *projection overlay relationship* $por(f_{fi}, f_{fj})$ means whether projected geometries of two fabrication features f_{fi} and f_{fj} onto a horizontal plane have a common region or not. It is formally defined as Eq.(4).

$$por(f_{fi}, f_{fj}) = \begin{cases} true & (prj(f_{fi}) \otimes prj(f_{fj}) \neq \emptyset) \\ false & (otherwise) \end{cases} \quad (4)$$

where, $prj(f_f)$ means that a 2D Boolean sum among projected shapes of all faces in a fabrication feature f_f onto a horizontal plane, $\otimes$ a 2D Boolean intersection of two planer shapes.

Based on the relation, we define a *projection overlay relationship matrix* $\mathbf{A}_{FF} = [a_{ij}]$ as Eq.(5).

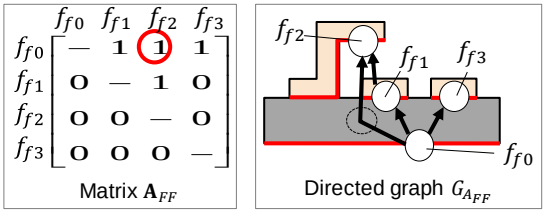
$$a_{ij} = \begin{cases} 1 & \left(\begin{array}{c} max\left[\left\{z\left(f^t(f_{fi})\right)\right\}\right] < max\left[\left\{z\left(f^t(f_{fj})\right)\right\}\right], \\ por(f_{fi},\ f_{fj}) = true \end{array}\right) \\ 0 & (por(f_{fi},\ f_{fj}) = false) \end{cases} \quad (5)$$

where $max\left[\left\{z\left(f^t(f_{fj})\right)\right\}\right]$ shows the maximum z value among *top faces* in a fabrication feature f_f. An example of the projection overlay relationship and its matrix representation is shown in **Fig.8**.

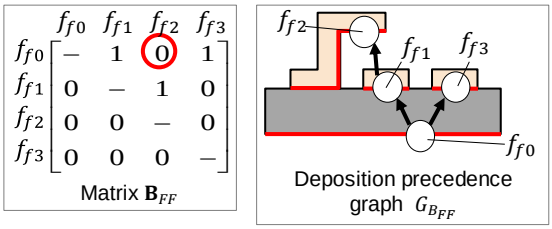
The projection overlay matrix $\mathbf{A}_{FF}$ implies the deposition precedence between two fabrication features. For example, a_{ij}=1 means that the feature f_{fi} has to be completed before the feature f_{fj}.

4.4 Generating the deposition precedence graph

From the projection overlay relation matrix, a *deposition precedence graph* is generated where the redundant deposition precedence among the fabrication



(a) Projection overlay relationship



(b) Deposition precedence

Figure 9 Projection overlay relationship and deposition precedence

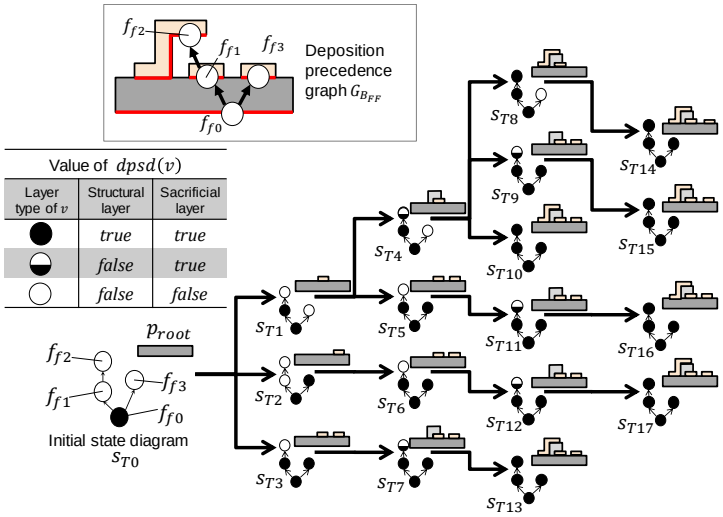


Figure 10 State diagram and process tree

features is removed.

The matrix $\mathbf{A}_{FF}$ represents a directed graph $G_{A_{FF}}$ whose nodes are fabrication features and whose directed arcs the deposition precedence between two features. In an example of **Fig.9**, a fabrication feature f_{f2} has two direct paren t nodes f_{f1} and f_{f0} in $G_{A_{FF}}$, and it means f_{f1} and f_{f0} must be deposited before f_{f2}. On the other hand, f_{f1} has the parent node f_{f0} which means f_{f0} must be made before f_{f1}. In this case, the directed arc (f_{f0}, f_{f2}) is considered to be redundant.

Similar to this case, if an arc e in $G_{A_{FF}}$ can be replaced with a directed walk longer than e, e is redundant and removed**.** By removing all redundant arcs from $G_{A_{FF}}$**,** a *deposition precedence graph* $G_{B_{FF}}$ and a *deposition precedence matrix* $\mathbf{B}_{FF}$ are obtained as Eq.6, where FF is a set of fabrication features.

$$G_{B_{FF}} = \langle FF,\ E_{FF} \rangle,$$
$$E_{FF} = \{(f_{fi}, f_{fj}) \mid f_{fi}, f_{fj} \in FF, b_{ij} = 1\} \quad (6)$$
$$\mathbf{B}_{FF} = [b_{ij}]$$

4.5 Generating a process tree

The deposition precedence matrix $\mathbf{B}_{FF}$ expresses the minimum required precedence for layer deposition, so feasible process sequences are exhaustively searched so that they comply with the precedence expressed by $\mathbf{B}_{FF}$. Multiple feasible process sequences can be discovered, and the results are summarized as a *process tree*.

For finding the feasible process sequences in the form of a process tree, we first introduced a new diagram called a *state diagram* S_T which is an extension of the deposition precedence graph $G_{B_{FF}}$. The state diagram explicitly expresses whether a structural and sacrificial layer is already made in a process sequence.

Before making an initial state diagramS_T, first, all fabrication features with an attribute value $sac_{pf}(f_{fj}) = true$ are selected from $G_{B_{FF}}$. It means that a sacrificial layer must be deposited right before the fabrication feature f_{fj} in structural layers. So, a new node f_{fj}^{s} expressing the sacrificial layer which temporarily contact with f_{fj} is inserted into $G_{B_{FF}}$ between the node f_{fj} and its parent node, and new edges are added correspondingly. Moreover, by adding a few attributes, an initial state diagram S_T is made as Eq.(7).

$$S_T = \langle V_T,\ E_T,\ dpsd,\ mat_f \rangle \quad (7)$$
$$V_T = FF \cup \{f_{fj}^{s}\}$$
$$E_T = \begin{matrix}\{(f_{fi}, f_{fj}) \mid b_{ij} = 1,\ sac(f_{fj}) = false\} \cup \\ \{(f_{fi}, f_{fj}) \mid b_{ij} = 1,\ sac(f_{fj}) = true\} \cup \\ \{(f_{fj}^{s}, f_{fj}) \mid sac(f_{fj}) = true\}\end{matrix}$$
$$dpsd: V_T \to \{true, false\},\quad mat_f: V_T \to M_n$$

where, V_T is a set of nodes of the state diagram whose element v virtually shows a structural or sacrificial layer, E_T a set of directed arcs of S_T, and $\{f_{fj}^{s}\}$ a set of the added sacrificial layers. $dpsd(v)$ shows whether a structural or sacrificial layer v has been already deposited. In the initial state diagram, the attribute is initialized as $dpsd(v) = true$ only for a substrate layer and $false$ for all other layers $v(\in V_T)$. Starting from this initial state, a process sequence can be obtained by changing the attribute value as $dpsd(v) = true$ layer by layer in S_T until all layers in V_T are assigned with $true$.

All feasible process sequences can be expressed a *process tree* P_R. As shown in **Fig.10**, its node is linked to different instances of the state diagram S_T where different attribute values of $dpsd(v)$ are assigned, and its arc shows the change in the layer deposition status in one process step. The process tree T_R is formally defined as Eq.(8).

$$T_R = \langle P_R,\ L_R,\ state \rangle \quad (8)$$

where P_R is a set of nodes of the tree, L_R a set of directed arcs (p_i, p_j) between two consecutive layer deposition states p_i and $p_j\ (\in P_R)$. An attribute $state: P_R \to S_T$ links a tree node to a state diagram instance $s_T(\in S_T)$. Different paths from the root node to

leaf nodes in P_R represent different feasible process sequences.

As shown in **Fig.10**, the process tree is generated according to the depth-first search of the following steps;

Step1: The initial state diagram s_{T0} is linked to a root node of the tree p_{root} as $state\,(p_{root}) = s_{T0}$. And set $p_{cur} \leftarrow p_{root}$.

Step2: If any set of nodes (layers) V_C which satisfies the following condition can be found in V_T of the state diagram $state\,(p_{cur})$, then proceed to Step 3. If no node in V_C is found, stop searching.

$$V_C = \left\{ v \;\middle|\; \begin{array}{l} u, v \in V_T, \quad (u, v) \in E_T \\ deposited(u) = true\,, \\ deposited(v) = false \end{array} \right\}$$

Step3: Take a subset of layers as $W_C \in 2^{V_C}$, where 2^{V_C} is a power set of V_C. For the subset W_C, the following tests (3a) and (3b) are executed sequentially.

(3a) If all layers $\forall w \in W_C$ are made of an identical material $mat_f(w)$, then assign $dpsd(w) = true$ for these layers to make a new instance s_{Tw} of the state diagram S_T. A new node p is created right below the node p_{cur} in P_R, and s_{Tw} is linked to the new node as $state\,(p) = s_{Tw}$. Finally, update $p_{prev} \leftarrow p_{cur}$, $p_{cur} \leftarrow p$.

(3b) If all layers $\forall x \in V_T$ in the original V_T have already assigned with $dpsd(x) = true$, then return to the previous node in the tree p_{prev}, and reset $p_{cur} \leftarrow p_{prev}$. And take the other subset of layers $W_C \in 2^{V_C}$, and repeat from Step2. Otherwise, simply repeat from Step2

By repeating the search, all feasible process sequences can be extracted from the device model, and a process tree P_R can be completed.

4.6 Extracting feasible process parameters

As a last stage of the process extraction, process parameters of every process step p_i in feasible process sequences are estimated. The parameters consist of

1) <u>A set of fabrication features</u> FF_p: $P_R \rightarrow 2^{FF}$
   Multiple fabrication features can be made in one process step $p_j\ (\in P_R)$ at the same time. So, they are stored as a set of the features $FF_p(p_j)(\subset FF)$.
2) <u>Layer type</u> $type_l$: $P_R \rightarrow \{str,\ sac\}$
   This attribute distinguishes whether the layer to be fabricated in p_j is a structural layer $type_l(p_j) = str$ or a sacrificial layer $type_l(p_j) = sac$.
3) <u>Material</u> (mat_p : $P_R \rightarrow M_n$)
   This attribute shows a material to be deposited or etched in p_j.
4) <u>Deposition thickness</u> t_{dep}: $P_R \rightarrow R^+$
   The deposition thickness t_{dep} in p_i is set to the minimum thickness among those of the fabrication features t_{pf} in $FF_p(p_i)$.
5) <u>Step coverage</u> a_{scf} : $P_R \rightarrow R^+$
   The ratio of a horizontal thickness to a vertical thickness of deposition is called *step coverage.* It depends on layer materials and equipment used in p_i. So it is treated as a user-defined constant, and $a_{scf}(p_i)$=1.0 is being used as a default value.
6) <u>Mask geometry</u> $mask$: $P_R \rightarrow G$
   The mask geometry $mask(p_i)$ is a kind of 2D planar pattern G generated by projecting a photoresist geometry and composed of a set of horizontal faces. The detail is described in 5.

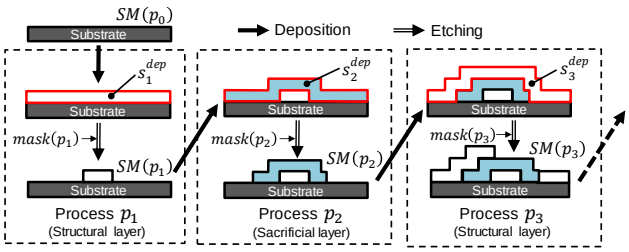


Figure 11 Estimating actual layer geometries

5. Geometry estimation function

Even if a feasible process can be found in the process extraction function, manufacturable device geometry may differ from the original device model due to the strong geometric limitation of MEMS process. So, in the geometry estimation function, a sequence of 3D device geometries actually created by a feasible process sequence is estimated using a solid modeler.

5.1 Estimating deposition layer geometries

Fig.11 shows how the function generates a sequence of actual 3D device geometries. The solid model of the device geometry $SM(p_i)$ made after a process step p_i $(i > 0)$ is expressed as

$$SM(p_i) = \langle S(p_i),\ F(p_i),\ E(p_i),\ mat_s \rangle$$

where $S(p_i)$ is a set of solid bodies of the layer remained at the end of the process step p_i, and $F(p_i)$ and $E(p_i)$ a set of faces and edges in $S(p_i)$.

The simulation proceeds in the forward direction of the process sequence. First, the solid model of the initial geometry $SM(p_0)$ is initialized so that $S(p_0)$ is set to be $\{s_0\}$, where $s_0 (\in S)$ is a solid body of a substrate.

In a general process step $p_i\ (i > 0)$, a solid body of the layer s_i^{dep} made in the deposition process p_i is estimated first. Then a solid body of the layer after the etching process in p_i using its mask geometry $mask(p_i) \in G$ is estimated next. As a result, the solid model of the device geometry $SM(p_i)$ at the end of the step p_i can be simulated. By repeating the simulation, a sequence of 3D device geometries created by a feasible process sequence can be obtained as a solid model which may be different from the initial device model SM_{init}

First, 3D geometry of a deposition layer in a step p_i is estimated from the fabrication feature geometries under the layer. First, as shown in **Fig.12(a)**, a set of all faces F^{surf} in $SM(p_{i-1})$ which are exposed outside are extracted by the following Boolean operation

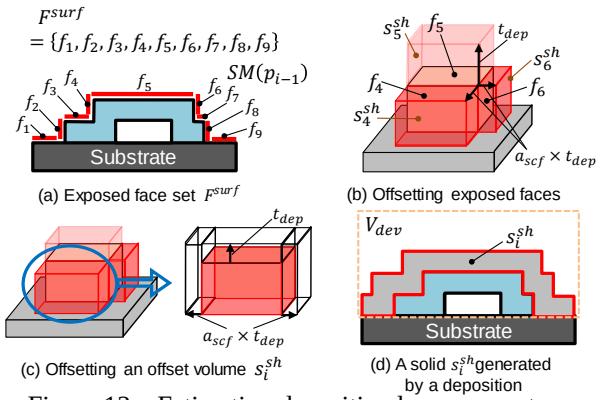


Figure 12 Estimating deposition layer geometry

of Eq.(9) in a solid modeler.

$$F^{surf} = \oplus_{f_i \in F(p_{i-1})} [\, f_i \ominus (F(p_{i-1}) - \{f_i\})] \qquad (9)$$

where $F(p_{i-1})$ is a set of faces included in $SM(p_{i-1})$, $\oplus$ 2D Boolean sum, $\ominus$ 2D Boolean difference two planer geometries, and $-$ normal difference set.

Then, shown in **Fig.12(b),** every face f_j in F^{surf} is offset along its normal direction $\boldsymbol{n}(f_j)$ to make a thin solid body s_j^{sh} based on Eq.(10).

$$s_j^{sh} = \begin{cases} swp\{f_j, \boldsymbol{n}(f_j), t_{dep}(p_i)\} & (\boldsymbol{n}(f_j) = +\boldsymbol{z}) \\ swp\{f_j, \boldsymbol{n}(f_j),\ a_{scf}(p_i) t_{dep}(p_i)\} & (\boldsymbol{n}(f_j) \perp +\boldsymbol{z}) \end{cases} \qquad (10)$$

where $swp\{f, \boldsymbol{n}, t\}$ is a solid body created by extruding a face f along its normal direction $\boldsymbol{n}$ with thickness t. Moreover as shown in **Fig.12(c)**, when $\boldsymbol{n}(f_j) \perp +\boldsymbol{z}$, a top face of s_j^{sh} is further offset along the vertical direction $+\boldsymbol{z}$ with distance $t_{dep}(p_i)$, and side faces of the s_j^{sh} is offset along their face normal with distance $a_{scf}(p_i) t_{dep}(p_i)$ respectively.

Finally, by taking the Boolean operation of Eq.(11), a solid body of the layer made by the deposition process s_i^{dep} can be estimated as shown in **Fig.12(d)**.

$$s_i^{dep} = \left[\left(\hat{\cup}_{f_j \in F^{surf}} s_j^{sh} \right) - S(p_{i-1}) \right] \hat{\cap}\, V_{dev} \qquad (11)$$

where $\hat{\cup}$ and $\hat{\cap}$ are 3D Boolean sum and intersection.

5.2 Calculating mask geometry

Etching is a material removal process, and geometry of photoresist masks must be designed so that the necessary portions of the layer remain after the etching. In this research, we assume that the positive photoresist is used where masked portions finally remain.

The mask geometry differs according to the layer type; structural or sacrificial. In case of the structural layer shown in **Fig13(a)**, the deposited layers which are placed right above a set of the fabrication features $FF_p(p_i)$ generated in a step p_i have to remain and to be masked. So the mask geometry $mask(p_i)$ can be created by Eq.(12).

$$mask(p_i) = proj\{FF_p(p_i)\} \qquad (12)$$

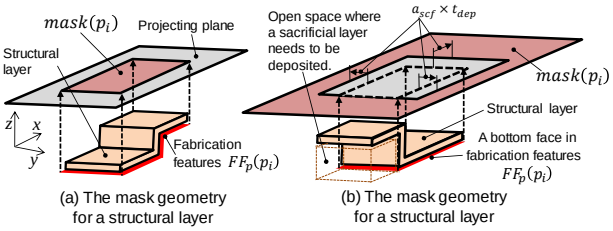


Figure 13 Calculating mask geometry

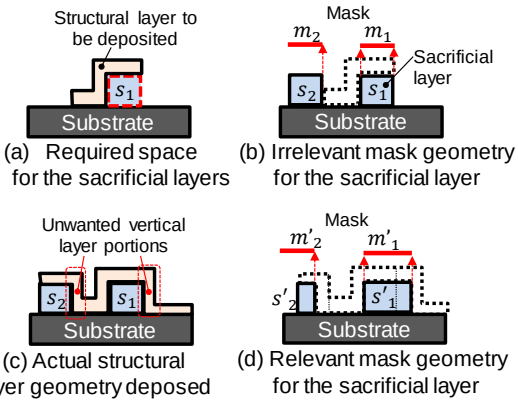


Figure 14 Relevant mask geometry for sacrificial layers

where $proj\{\}$ means a projection operator onto a horizontal plane.

On the other hand, in case of the sacrificial layer, its mask calculation is a little complicated. For example, the sacrificial layers needed for making the other structural layer shown in **Fig.14(a)** must be placed at a space s_1 and s_2 in **Fig.14(b)**, and the masks for making s_1 and s_2 are first estimated as m_1 and m_2 in **Fig.14(b)**. However, when using m_1 and m_2 directly, unwanted vertical layer portions of the structural layer are made on the sidewalls of s_1 and s_2 as shown in **Fig.14(c**), and they are unable to remove afterward. So, the sacrificial layer needs to remain so as to avoid depositing a deep structural layer on the sidewalls and to be covered with the extended masks m'_1 and m'_2 as shown in **Fig.14(d**).

As a result, the mask geometry for the sacrificial layer $mask(p_i)$ is calculated by projecting extended bottom face of the fabrication feature using Eq.(13).

$$mask(p_i) = f_0 \hat{-} proj\left\{ ofst\left(FF_p^{bt}(p_i), a_{scf}(p_i) t_{dep}(p_i) \right) \right\} \qquad (13)$$

where f_0 is an upward horizontal substrate surface, and $FF_p^{bt}(p_i)$ a set of the top and bottom faces which are in fabrication features $FF_p(p_i)$ and do not have an open space in the device side. As shown in **Fig.13(b)**, $ofst(FF, d)$ shows an offset operator for the boundaries of the 2D face FF with a distance d. $\hat{-}$ is a 3D Boolean difference.

5.3 Estimating the etched area

Finally the volume removed by etching process is estimated using the mask geometries. The volume protected by the mask in a process step p_i is composed both of a volume S_i^{mask} masked by the photoresist and of $S_i^{o\_mat}$ completely covered and closed by the other material layers. The projected volumes can be

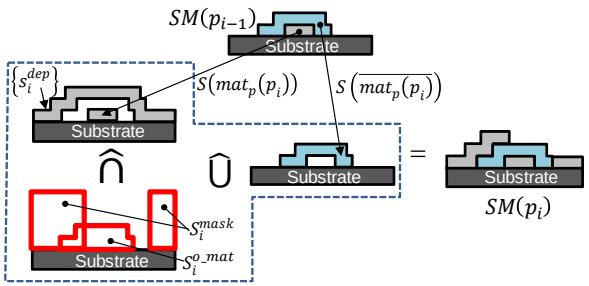


Figure 15 Boolean operations
for estimating actual device geometry

respectively calculated using the sweeping operation of Eqs.(14,15) .

$$S_i^{mask} = \{s_j \mid s_j = swp(m_k, +\mathbf{z}, \alpha), m_k \in mask(p_i)\} \quad (14)$$

$$S_i^{o\_mat} = \begin{Bmatrix} s_j \mid s_j = swp(f_l, -\mathbf{z}, \alpha), f_l \in F_{om}(s_l) \\ mat_s(s_l) \neq mat_e(p_i),\ s_l \in S(p_i) \end{Bmatrix} \cap V_{dev} \quad (15)$$

where, s_l is a solid body of the layer made from a material which is not be removed by the etching process p_i, $mat_e(p_i)$ a martial to be etched in p_i, and $F_{om}(s_l)$ is a set of horizontal faces with a normal of $+\mathbf{z}$ in the solid body of the layer s_l, and α is a length larger than the maximum height of the final device.

As shown in **Fig.15**, a new device geometry $S(p_i)$ after the deposition and etching in p_i is estimated from by taking a combined Boolean operations of Eq.(16) among the previous device geometry $SM(p_{i-1})$, S_i^{mask} and $S_i^{o\_mat}$ as,

$$S(p_i) = \begin{bmatrix} \left\{\{s_i^{dep}\} \cup S\left(mat_p(p_i)\right)\right\} \widehat{\cap} \\ \{S_i^{mask} \cup S_i^{o\_mat}\} \end{bmatrix} \widehat{\cup} S(\overline{mat_p(p_i)}) \quad (16)$$

where, $S\left(mat_p(p_i)\right)$ is a set of solid bodies in $SM(p_{i-1})$ whose material is identical to the one $mat_p(p_i)$ used in the deposition and etching of p_i, and $S(\overline{mat_p(p_i)})$ a set of solid bodies whose material is different from $mat_p(p_i)$.

In the operation of Eq.(16), the solid bodies with a deposition material are added, and the bodies with an etched material removed. By repeating these operations in the solid model, change in device model geometry in a feasible process sequence is obtained except for the sacrificial layer removal by an etching. Finally, the solid bodies of the sacrificial layers exposed outside are deleted to simulate the sacrificial layer etching.

6. Associative modification function

6.1 Objective of the function

The feasible device geometry simulated by the geometry estimation function might differ from the one of the original device model and does not necessarily satisfy the original performance specification such as electric capacity or resonant frequency. In that case, the simulated device geometry has to be revised so as to satisfy the original specification while keeping the manufacturability of the device.

To support the consistent revision, an associative modification function is developed. The process parameters of a feasible process sequence are linked to several dimensional parameters of the device model (so called *device parameters*). Once the links are defined, the process parameters can be automatically revised only by changing the device parameters. And the process parameters where the device geometry satisfies both the original specification and the manufacturability can be found.

6.2 Associative modification between device and process parameters

For the modification, the feasible device model $SM(p_i)$ is linked to a *layer model* $LM(p_i)$ of Eq.(17) to clarify the process parameters of a layer generated in a process step p_i explicitly.

$$LM(p_i) = \langle L(p_i), S(p_i), F(p_i), E(p_i), mat_l \rangle \quad (17)$$
$$l(p_i) = \langle t_{dep}(p_i), mask(p_i), a_{scf}(p_i) \rangle \ (\in L(p_i))$$

where, $L(p_i)$ is a set of the *process parameters* of deposited layers, and $l(p_i)$ the *process parameters* defining the layer geometry made in p_i.

As shown in **Fig.16(a)** , if $F(s(p_i))$ denotes a set of faces which make up a layer $s(p_i)(\in S(p_i))$, then $F(s(p_i))$ is classified into the following three subsets.

$$F_{xy}(s(p_i)) = \{f_j \mid f_j \in F(s(p_i)), \mathbf{n}(f_j) = +\mathbf{z}\}$$
$$F_s(s(p_i)) = \{f_j \mid f_j \in F(s(p_i)), \mathbf{n}(f_j) = \perp \mathbf{z},\ E_v(f_j) = \phi\}$$
$$F_w(s(p_i)) = \{f_j \mid f_j \in F(s(p_i)), \mathbf{n}(f_j) = \perp \mathbf{z},\ E_v(f_j) \neq \phi\}$$

where, $E_v(f_j)$ is a set of concave edges placed at the boundary of f_j.

The layer geometry $s(p_i)$ is completely controlled only by three process parameters $l(p_i)$; deposition thickness $t_{dep}(p_i)$, mask geometry $mask(p_i)$ and step-coverage $a_{scf}(p_i)$. The deposition thickness can be easily controlled by changing the deposition time of p_i in the equipment. The step coverage can be changed by changing the deposited material and its equipment. Therefore, we assume that these three process parameters are linked to the device parameters and can be changed in conjunction with the change in the device parameters.

So, only the geometry of the faces in **Fig.22(a)** $F_{xy}(s(p_i))$, $F_s(s(p_i))$ or $F_w(s(p_i))$ are allowed to be offset as the changes in the device parameters shown in **Fig.16**, and the process parameters are re-evaluated in conjunction with the offset. Finally, the

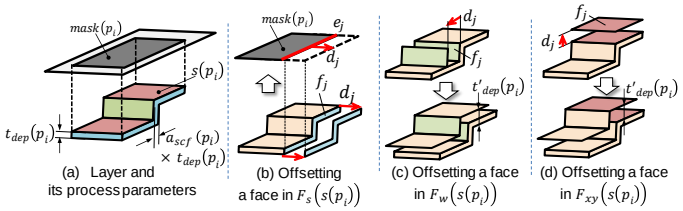


Figure 16 Modification of device parameters

modified geometry based on the revised process parameters is simulated again in the geometry estimation function.

When offsetting a face by a distance d_k in device, the process parameters are modified as follows;

1) Offsetting a face in $F_s(s(p_i))$

As shown in **Fig.16(b)**, offsetting a face f_j in $F_s(s(p_i))$by d_j results in offsetting the corresponding 2D edge e_j of the mask by d_j.

2) Offsetting the faces in $F_w(s(p_i))$

As shown in **Fig.16(c)**, offsetting the face f_j in $F_w(s(p_i))$ by d_j causes the changes in the side wall thickness of the layer. This eventually results in change in the deposition thickness from $t_{dep}(p_i)$ to $t'_{dep}(p_i)$ as $t'_{dep}(p_i) = t_{dep}(p_i) + d_j/a_{scf}(p_i)$, where a_{scf} is the defined step coverage. At the same time, it also enforces the faces $F_{xy}(l(p_i))$ to be offset by $d_j/a_{scf}(p_i)$.

3) Offsetting the faces in $F_{xy}(s(p_i))$

As shown in **Fig.16(d)**, offsetting the face f_j in $F_{xy}(s(p_i))$ by d_j causes the changes in vertical thickness of the layer. As a result, the deposition thickness d_j needs to be changed from $t_{dep}(p_i)$ to $t'_{dep}(p_i)$ as $t'_{dep}(p_i) = t_{dep}(p_i) + d_j$. Similar to 2), it also enforces the other faces in $F_w(s(p_i))$ to be offset by $d_j/a_{scf}(p_i)$.

7. Case studies

7.1 Process planning of a micro oxide sensor

The proposed process planning system was implemented using a solid modeling kernel (Parasolid) and our own code of C++.

First feasible process plans of a micro-oxide-sensor[9] whose initial device model is shown in **Fig.17** were discovered by the process extraction function and geometry estimation function, and were verified by the other commercial MEMS process emulation software. The sensor is composed of layers made of Si_3N_4, Pt and ZrO_2. A micro chamber structure with a very small orifice is made of Si_3N_4. The device model consists of five solid bodies of the layers. In the process extraction function, 46 process features and 9 fabrication features including the substrate feature were found in 17 sec using a standard PC. As a result three different feasible process sequences were derived.

Among them, a feasible process with minimum process steps is summarized in **Fig.18** which includes one sacrificial layer deposition is needed. The mask geometries used in the process are also shown in **Fig.18**. The etching is not needed in p_1, so the mask geometry is blacked out. Using the geometry estimation function, the sequence of manufacturable geometries of the micro-sensor corresponding to the selected process is also estimated as **Fig.19**. The estimation took only 1 sec. As a result, it was found that several portions of the manufacturable geometries differed from those of the initial device as shown in **Fig.20(a)** but that the geometry of the wiring, electrodes and orifice seemed to be correctly realized.

Finally, the validity of the process plan derived from

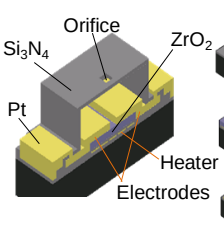


Figure 17 Initial device model of a micro-oxide-sensor

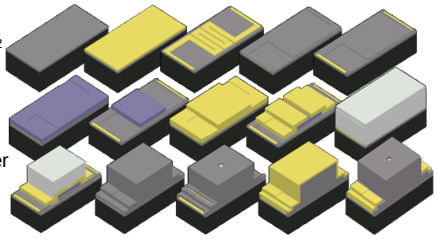
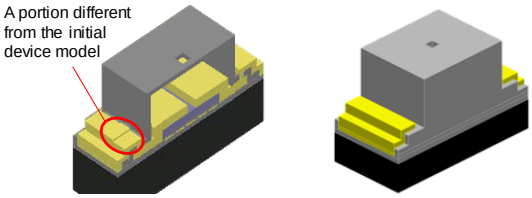


Figure 19 A sequence of manufacturable device geometries in a feasible process

Process step	Fabrication features	mat_p	t_{dep}	$mask$	a_{scf}	$type_l$
p_1	f_{f1}	Si_3N_4	0.05	-	1.0	str
p_2	f_{f2}	Pt	0.02	Mask2	1.0	str
p_3	f_{f3}	SiO2	0.02	Mask3	1.0	str
p_4	f_{f4}	ZrO_2	0.1	Mask4	1.0	str
p_5	f_{f5} , f_{f6}	Pt	0.1	Mask5	1.0	str
p_6	f_{f7}	SiO2	0.45	Mask6	1.0	sac
p_7	f_{f7}	Si_3N_4	0.05	Mask7	1.0	str
p_8	f_{f8}	Pt	0.05	Mask8	1.0	str
p_9	Sacrificial layer removal					

Figure 18 The process parameters and the mask geometries of a feasible process model



(a) The manufacturable device model derived from our planning system

(b) The manufacturable device model estimated from a commercial process emulator[6]

Figure 20 Comparison of the manufacturable device geometries

our system was verified. In the verification, the derived plan with the mask geometries was input into a commercial MEMS process emulator MEMS-One[6] where change of 3D geometries of the device model can be simulated along forward direction according to the process. Then the device model geometries from the MEMS-one shown in **Fig.20(b)** was compared with those from our system in **Fig.20(a)**. As a result, we confirmed that both geometries substantially agreed. Moreover, the examination by MEMS expert researchers validated that the process sequences obtained in the system were completely feasible and plausible.

7.2 Associative redesign of a micro hinge

On the other hand, we verified the effectiveness of the associative modification function by the process planning and redesign of a *micro-hinge* device. The initial device model of the hinge is shown in **Fig.21(a)**. The hinge part must be able to rotate about an axis and is used for setting up a micro lens.

In process estimation function, only one feasible

process plan was derived in 0.4 sec, and the manufacturable hinge geometry was estimated as in the geometry estimation function shown in **Fig.21(b)**. The estimated manufacturable device geometry resembles the initial one to some extent, but differs from the initial one in the portion indicated by a red circle.

We assumed that the estimated device geometry will no longer satisfy the design specification, and modified the geometry using the associative modification function. Two modification cases were verified. In the first case, the width of the hinge was enlarged shown in **Fig.22**. Then the mask geometry in a process step was automatically changed, and the final device model was changed as shown in **Fig.22(a)**. In the second case, the axis portion was trimmed so as to keep enough space to rotate. Similar to the first case, the mask geometries in two process steps and a deposition thickness were changed, and the final device model was modified as shown in **Fig.22(b)** according to the revision.

From these examples, we confirmed that the device parameters and process parameters were adequately linked and could be changed simultaneously while keeping the fabrication constraints.

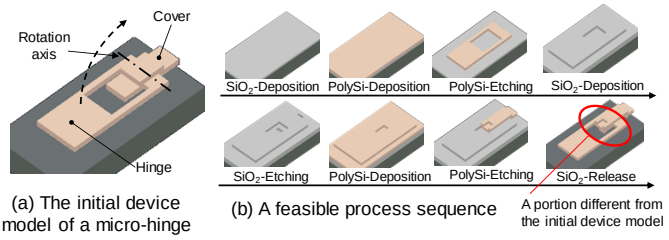


Figure 21 Device models of a micro-hinge

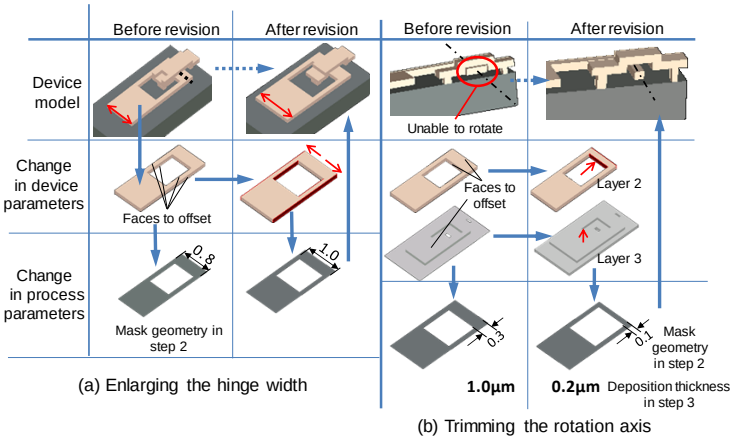


Figure 22 Associative modification between device parameters and process parameters

8. Conclusion

A new process planning system for MEMS devices for non-expert MEMS designers was developed. In the system, all feasible fabrication processes could be exhaustively derived from a 3D MEMS device model, and 3D geometries of the device actually manufactured by the derived process could be simulated. Moreover, the original process parameters such as mask geometries and deposition thickness could be automatically revised according to the redesign of dimensional parameters of the device. A process planning for a micro oxide sensor and a micro hinge were examined by the commercial MEMS process emulator and the results indicated that the derived process plans and estimated the device model geometry by the proposed system were plausible and effective.

However, in our system, the detailed geometry of layers in devices were still simplified as a set of flat planes despite that the actual geometry of the layer consists of curved surfaces generated by the photolithography-based fabrications. The issue will be solved as our future work.

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